We claim:

Sub A1

1. A memory interface device for interfacing a number of host applications to a memory device, the memory interface device comprising:

a host interface for interfacing with the number of host applications;

a memory interface for interfacing with the memory device;

a number of contexts operably coupled to the host interface for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications; and

control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications, and provide the result/status information to the number of host applications via the number of contexts.

2. The memory interface device of claim 1, wherein the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface.

3. The memory interface device of claim 1, wherein the memory device comprises a content-addressable memory (CAM), and wherein the memory interface conforms to a CAM interface.

4. The memory interface device of claim 1, wherein the number of contexts comprises a number of context registers sets.

5. The memory interface device of claim 4, wherein each context register set corresponds to one and only one of the number of host applications.

6. The memory interface device of claim 1, wherein the control logic comprises:

monitoring logic;

scheduling logic;

memory interface logic; and

result/status logic, wherein:

the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic;

the scheduling logic is operably coupled to schedule memory access operations for the memory access requests;

the memory interface logic is operably coupled to generate memory interface signals for interfacing with the memory device over the memory interface; and

the result/status logic is operably coupled to provide result/status information to the number of host application(s).

7. The memory interface device of claim 6, wherein each context comprises a context register set, and wherein the monitoring logic is operably coupled to monitor a predetermined register in each context register set to detect a memory access request.

8. The memory interface device of claim 7, wherein the predetermined register comprises an instruction register.

9. The memory interface device of claim 6, wherein the memory interface supports pipelining of memory access operations, and wherein the scheduling logic is operably coupled to pipeline a plurality of memory access requests over the memory interface.

10. The memory interface device of claim 9, wherein the scheduling logic is operably coupled to determine that a plurality of memory access requests conflict and execute at least one of the conflicting memory access requests as an atomic operation.

11. The memory interface device of claim 10, wherein the scheduling logic is operably coupled to clear the pipeline in order to execute the conflicting memory access request as an atomic operation.

12. The memory interface device of claim 6, wherein the result/status logic is operably coupled to correlate result/status information with its corresponding memory access request.

13. The memory interface device of claim 6, wherein the result/status logic is operably coupled to store the result/status information for each memory access request in a corresponding context.

14. The memory interface device of claim 13, wherein each context comprises a validity indicator, and wherein the result/status logic is operably coupled to set the validity indicator in each context when the corresponding memory access is complete and the result/status information is available.

15. The memory interface device of claim 1 embodied as programmed programmable logic device.

16. The memory interface device of claim 1 embodied as an application specific integrated circuit.

Sub #2

17. Program logic for programming a programmable logic device, the program logic comprising:

host interface logic for interfacing with the number of host applications;

memory interface logic for interfacing with the memory device;

a number of contexts operably coupled to the host interface logic for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications; and

control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device using the memory interface logic for servicing the memory access requests on behalf of the number of host applications, and provide the result/status information to the number of host applications via the number of contexts.

18. The program logic of claim 17, wherein the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface logic conforms to a packet processor interface.

19. The program logic of claim 17, wherein the memory device comprises a content-addressable memory (CAM), and wherein the memory interface logic conforms to a CAM interface.

20. The program logic of claim 17, wherein the number of contexts comprises a number of context registers sets.

21. The program logic of claim 20, wherein each context register set corresponds to one and only one of the number of host applications.

22. The program logic of claim 17, wherein the control logic comprises:

monitoring logic;

scheduling logic;

memory interface logic; and

result/status logic, wherein:

the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic;

the scheduling logic is operably coupled to schedule memory access operations for the memory access requests;

the memory interface logic is operably coupled to generate memory interface signals for interfacing with the memory device using the memory interface logic; and

the result/status logic is operably coupled to provide result/status information to the number of host application(s).

23. The program logic of claim 22, wherein each context comprises a context register set, and wherein the monitoring logic is operably coupled to monitor a predetermined register in each context register set to detect a memory access request.

24. The program logic of claim 23, wherein the predetermined register comprises an instruction register.

25. The program logic of claim 22, wherein the memory interface supports pipelining of memory access operations, and wherein the scheduling logic is operably coupled to pipeline a plurality of memory access requests over the memory interface.

26. The program logic of claim 25, wherein the scheduling logic is operably coupled to determine that a plurality of memory access requests conflict and execute at least one of the conflicting memory access requests as an atomic operation.

27. The program logic of claim 26, wherein the scheduling logic is operably coupled to clear the pipeline in order to execute the conflicting memory access request as an atomic operation.

28. The program logic of claim 22, wherein the result/status logic is operably coupled to correlate result/status information with its corresponding memory access request.

29. The program logic of claim 22, wherein the result/status logic is operably coupled to store the result/status information for each memory access request in a corresponding context.

30. The program logic of claim 29, wherein each context comprises a validity indicator, and wherein the result/status logic is operably coupled to set the validity indicator in each context when the corresponding memory access is complete and the result/status information is available.

31. The program logic of claim 17 embodied in a computer readable medium.

Sub A3

32. An apparatus comprising:

a number of host applications;

a memory device; and

a memory interface device interposed between the host applications and the memory device and operably coupled to receive memory access requests from the number of host applications, interact with the memory device on behalf of the number of host applications for servicing the memory access requests, and provide result/status information to the host applications.

33. The apparatus of claim 32, wherein the memory interface device comprises:

a host interface for interfacing with the number of host applications;

a memory interface for interfacing with the memory device;

a number of contexts operably coupled to the host interface for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications; and

control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications, and provide the result/status information to the number of host applications via the number of contexts.

34. The apparatus of claim 33, wherein the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface.

35. The apparatus of claim 33, wherein the memory device comprises a content-addressable memory (CAM), and wherein the memory interface conforms to a CAM interface.

36. The apparatus of claim 33, wherein the number of contexts comprises a number of context registers sets.

37. The apparatus of claim 36, wherein each context register set corresponds to one and only one of the number of host applications.

38. The apparatus of claim 33, wherein the control logic comprises:

monitoring logic;

scheduling logic;

memory interface logic; and

result/status logic, wherein:

the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic;

the scheduling logic is operably coupled to schedule memory access operations for the memory access requests;

the memory interface logic is operably coupled to generate memory interface signals for interfacing with the memory device over the memory interface; and

the result/status logic is operably coupled to provide result/status information to the number of host application(s).

39. The apparatus of claim 38, wherein each context comprises a context register set, and wherein the monitoring logic is operably coupled to monitor a predetermined register in each context register set to detect a memory access request.

40. The apparatus of claim 39, wherein the predetermined register comprises an instruction register.

41. The apparatus of claim 38, wherein the memory interface supports pipelining of memory access operations, and wherein the scheduling logic is

operably coupled to pipeline a plurality of memory access requests over the memory interface.

42. The apparatus of claim 41, wherein the scheduling logic is operably coupled to determine that a plurality of memory access requests conflict and execute at least one of the conflicting memory access requests as an atomic operation.

43. The apparatus of claim 42, wherein the scheduling logic is operably coupled to clear the pipeline in order to execute the conflicting memory access request as an atomic operation.

44. The apparatus of claim 38, wherein the result/status logic is operably coupled to correlate result/status information with its corresponding memory access request.

45. The apparatus of claim 38, wherein the result/status logic is operably coupled to store the result/status information for each memory access request in a corresponding context.

46. The apparatus of claim 45, wherein each context comprises a validity indicator, and wherein the result/status logic is operably coupled to set the validity indicator in each context when the corresponding memory access is complete and the result/status information is available.

47. The apparatus of claim 32, wherein the memory interface device is a programmed programmable logic device.

48. The apparatus of claim 32, wherein the memory interface device is an application specific integrated circuit.